In the Claims

1. - 16. (canceled)

17. (original) A semiconductor device comprising:

a patterned deposited dielectric layer comprising a plurality of recesses therein;

a capacitor bottom plate formed within said recess;

an inhibitor layer covering only an upper region of said capacitor bottom plate such that a lower region of said capacitor bottom plate is not covered by said inhibitor layer, wherein said upper region of said capacitor bottom plate is smooth polysilicon and said lower region of said capacitor bottom plate is roughened polysilicon;

a capacitor cell dielectric layer formed over said inhibitor layer and over said bottom plate; and

a capacitor top plate layer formed over said cell dielectric layer, over said inhibitor layer, and over said capacitor bottom plate.

18. (original) The semiconductor device of claim 17, wherein:

said lower region of said capacitor bottom plate is hemispherical silicon grain (HSG) polysilicon;

said upper region of said capacitor bottom plate is smooth polysilicon; and

said inhibitor layer is oxide.

19. (original) The semiconductor device of claim 18 wherein said inhibitor layer is low silane flow oxide.

20. (original) The semiconductor device of claim 18 wherein said inhibitor layer is nitride.

21. (presently amended) A semiconductor device comprising:

a conductive container capacitor bottom plate layer comprising a single polysilicon layer;

a first portion of said bottom plate layer which defines a receptacle, wherein said first portion of said bottom plate layer comprises a first texture;

a second portion of said bottom plate layer which defines a rim to an interior of said receptacle, wherein said second portion of said bottom plate layer comprises a second texture which is smoother than said first texture; and

a cell dielectric layer formed over said bottom plate layer which contacts said first portion and said second portion of said bottom plate layer.

22. (canceled)

23. (presently amended) The semiconductor device of claim ~~22~~ 21, wherein:

said first portion of said container capacitor bottom plate layer is hemispherical silicon grain (HSG) polysilicon; and

said second portion of said container capacitor bottom plate layer is smooth polysilicon.

24. (previously presented) A semiconductor device comprising a container capacitor, said container capacitor comprising:

a capacitor bottom plate having a bottom and an inside which together define a receptacle, a rim which defines an opening to an interior of said receptacle, and an outside;

an inhibitor layer is on said bottom and on said rim of said capacitor bottom plate, wherein said bottom and said rim of said capacitor bottom plate have a first texture and said inside of said capacitor bottom plate has a second texture which is rougher than said first texture;

a capacitor cell dielectric is on said inhibitor layer on said bottom and said rim of said capacitor bottom plate, on said inside of said capacitor bottom plate, and over said outside of said capacitor bottom plate; and

a capacitor top plate formed on said cell dielectric layer.

25. (previously presented) The semiconductor device of claim 24 further comprising a dielectric layer which covers said outside of said capacitor bottom plate, wherein said outside of said bottom plate has said first texture.

26. (previously presented) The semiconductor device of claim 24 wherein said cell dielectric layer contacts a majority of said outside of said capacitor bottom plate, and said majority of said outside of said capacitor bottom plate has said second texture.